Adesh Bhor

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University of Oklahoma, Norman, OK
M.S. Electrical Engineering, GPA: 3.8, Graduated May 2026 | B.S. Electrical Engineering, GPA: 3.56
Thesis: A Hybrid Leaky Integrate-and-Fire Neuron with Tunable Reset Behavior in 7 nm Fin Field-Effect Transistor Technology

Summary: Electrical engineering professional with experience across circuit simulation, FPGA validation, PCB workflows, embedded interfaces, prototype PCBA manufacturing, and controls projects. Raised FPGA pipeline throughput by 30%, enabled approximately 30,000 additional SMT placements/day, and built repeatable analysis workflows across 6+ operating variables for engineering review.

EXPERIENCE

Graduate Research Assistant - Semiconductor Circuits, Hardware Validation & FPGA Systems *Apr 2023 - May 2026*
Gallogly College of Engineering, University of Oklahoma

- Characterized 7 nm FinFET CMOS circuit behavior across reset, firing frequency, power, energy, and robustness using Xschem/ngspice simulation and ASAP7 models.
- Automated multi-variable simulation sweeps and Python post-processing across 6+ operating variables, standardizing waveform comparisons and design-tradeoff reviews.
- Raised FPGA image-classification throughput by 30% by resolving timing-closure failures, implementation constraints, and hardware/software interface bottlenecks.
- Diagnosed mixed-signal sensitivity across biasing, supply, capacitance, and noise conditions, documenting findings for technical reviews and debug decisions.

Electronics Manufacturing Intern - Prototype PCBA Build, Test & SMT Support *Jun 2024 - Jul 2024*
GM Electronics

- Coordinated contractor build requirements, order expectations, and delivery timing while executing prototype PCBA build support, in-process test checks, final QC, defect logging, and corrective-action tracking.
- Optimized JUKI RS-1R feeder mapping, nozzle selection, component setup, and vision settings, enabling approximately 30,000 additional placements/day and saving approximately 1 hour/day.
- Standardized SMT setup and changeover documentation in a QMS/5S manufacturing environment, contributing to approximately 11% daily production efficiency gain.

Product Design Intern - Electromechanical Prototyping & Validation *Aug 2023 - Dec 2023*
Ronnie K. Irani Center for the Creation of Economic Wealth

- Raised prototype measurement accuracy by 40% by leading 60+ user interviews and validation tests to diagnose sensor limitations and guide design revisions.
- Applied sensor test data and stakeholder feedback across prototype iterations to improve manufacturability, usability, and reliability.

PROJECT EXPERIENCE

Altium PCB Design and Manufacturing Release Projects *Aug 2025 - Dec 2025*
Altium Designer, Schematic Capture, PCB Layout, ERC/DRC, Gerber/Drill, BOM, DFM

- Designed through-hole/SMD astable multivibrator PCBs and an iVCCSG2 self-powered IoT sensor-node PCB layout, producing custom libraries, ERC/DRC checks, Gerber/drill files, BOMs, and assembly documentation.

Air Compressor Monitoring System - USPS *Jan 2024 - May 2024*
Raspberry Pi, Python, RS-485/Modbus RTU, ADS1115, Streamlit, Plotly

- Designed a distributed monitoring system with 6+ RS-485 sensor nodes, ADC interfaces, Modbus RTU communication, alarms, and dashboards, cutting compressor downtime by 20%.

Autonomous Plant Care System *Jan 2025 - May 2025*
CLICK PLC, Ladder Logic, Relay-Based Control, Discrete Sensors

- Programmed and validated CLICK PLC ladder logic for sensor-driven relay control, including wiring checks, I/O validation, safety interlocks, and output response verification.

CORE COMPETENCIES

Hardware/Electrical Debug: Circuit troubleshooting, waveform capture, failure isolation, root-cause analysis, oscilloscopes, DMMs, bench power supplies, function generators

Design/EDA: Altium Designer, schematic capture, PCB layout, ERC/DRC, Gerber/drill/BOM outputs, Xschem, ngspice, ASAP7 FinFET models

Embedded/Controls Interfaces: FPGA validation, Vivado/Quartus timing closure, Python/MATLAB analysis, UART/SPI/I2C, RS-485/Modbus RTU, CLICK PLC